Lab #1: 8-bit Adder

EECE 2323 – Prof. Xiaolin Xu

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1. **Background & Purpose**

The objective of this lab is to create an 8-bit adder with output overflow flag in Verilog and simulate/test in the Xilinix platform, then generate a bitstream to be tested on the TUL PYNQ board and display the results on the LEDs. Each LED represents one single bit of outputs. The goal is to get familiar with the Verilog hardware how to implement module and how to test its correctness by reading its waveform. The Verilog and testbench code are written in Xilinix software. In this lab, the Xilinx Vivado software was introduced and used to design an 8-bit adder module using structural model. Vivado is one of the main software used in the design of logic circuits, and this lab shows the students how to use it to design simple logic circuits. The 8-bit adder adds the numbers digit by digit. It has two 8-bit inputs and outputs the sum of the inputs and the carry out flag.

1. **Prelab**
2. Complete the table below for the expected input and output values for the 8 bit adder circuit you are describing in lab 1. Note that the syntax used for constant values is from Verilog; a,b and f are two’s complement number.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| a | binary\_a | b | binary\_b | f | binary\_f | ovf |
| 8’d0 | 0000 0000 | 8’d0 | 0000 0000 | 8’d0 | 0000 0000 | 1’d0 |
| 8’d12 | 0000 1100 | 8’d34 | 00100010 | 8’d46 | 00101110 | 1’d0 |
| -8’d12 | 1111 0100 | -8’d34 | 11011110 | -8’d46 | 11010010 | 1’d0 |
| 8’d100 | 0110 0100 | -8’d50 | 11001110 | 8’d50 | 00110010 | 1’d0 |
| -8’d100 | 1001 1100 | 8’d50 | 00110010 | -8’d50 | 11001110 | 1’d0 |
| 8’d100 | 0110 0100 | 8’d100 | 0110 0100 | -8’d56 | 11001000 | 1’d1 |
| -8’d100 | 1001 1100 | -8’d100 | 1001 1100 | 8’d56 | 00111000 | 1’d1 |

1. Write a Boolean or verilog equation for the overflow output ovf based on input values a and b. Your equation can also incorporate output f.

assign ovf = (a[7] & b[7] & ~f[7]) | (~a[7] & ~b[7] & f[7)

1. A good simulation testbench tests that every input and output bit can take the values zero and one. For the values in question 1 answer the following questions:  
   (a) The adder has 16 bits of input and 9 bits of output. Do the values in question 1 taken together set every input bit to both one and zero and every output bit to both one and zero? Explain your answer. Identify which bits are not tested in this manner.

They do not set every input bit to both one and zero and every output bit to both one and zero. The test cases above have a[1:0] and b[0] all zeros. And it does not cover all outputs. The above test cases have outputs f[0] all zeros as well.

(b) Add additional input (a and b) values that test every bit in both the inputs and outputs so that every bit takes either a zero or a one value in your test cases.

a = 8’d3 = 8’b0000\_0011, b = 8’d0, f = 8’d3 = 8’b0000\_0011, ovf = 1’d0

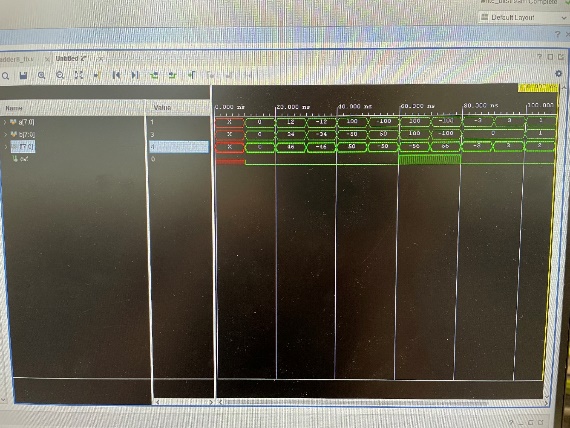
a = -8’d3 = 8’b1111\_1101, b = 8’d0, f = -8’d3, ovf = 1’d0

a = 8’d1 = 8’b0000\_0001, b = 8’d1, f = 8’d2 = 8’b0000\_0010, ovf = 1’d0

1. **Results and Analysis**

8-bit adder contained two 8-bit data inputs, one 8-bit data output and one overflow flag output. According to testbench simulation results, an 8-bit adder adds the number digit by digit. In simulation waveform, integers represent input a and b, respectively, and the resulting output is the sum a + b.

Appendix below showed the software simulation of the 8-bit adder testbench. The following tests demonstrated that the adder module correctly handles 8-bit inputs add operation.



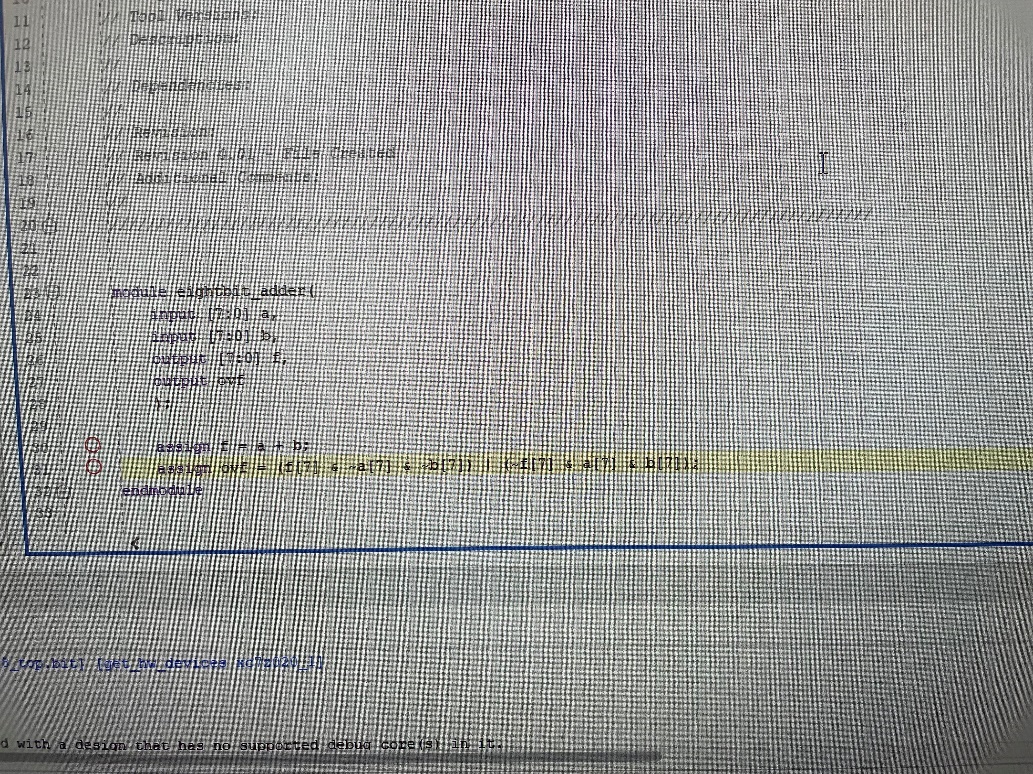
Appendix C: 8-bit Adder testbench simulation waveform

The 8-bit adder is the most common circuit module that is used in real digital systems a lot. By observing the simulation waveform, an overflow can be observed when the sum of the inputs is out of range from – 27 to 27. Once an overflow flag set, it indicates the output f itself does not make any sense to the computer anymore. Besides, it can be observed that two’s complement addition can be successfully calculated by computer using an adder. The output has some delay when input signals change. The delay is caused by addition operation and ovf must wait until the result of sum been calculated. The delay might be shortened in the future advanced implementation by isolating the calculation of sum and overflow.

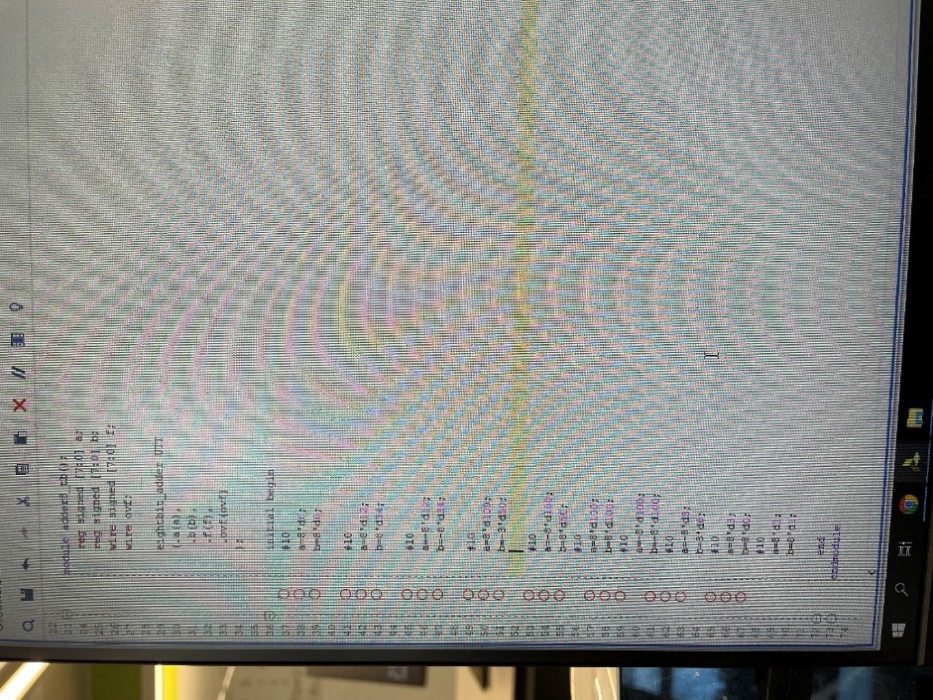
1. **Conclusion & Recommendations**

The lab objective is to create an 8-bit adder with overflow flag using Verilog and stimulated logic circuit with testbench. The implementation of the logic adder on the TUL PYNQ board successfully. demonstrates the add operations. The practice of Vivado software and programming skills lead to better understanding for future labs and tests. Based on the results of the simulation, it is necessary to experiment with more than 7 test values including the pre-lab's expected input and output table to comprehensively certify accurate behavior of the design.

1. **Appendices**

Appendix A: 8-bit Adder Module

Appendix B: 8-bit Adder testbench



Appendix C: 8-bit Adder testbench simulation waveform